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1 Analog IP Testing: Diagnosis and Optimization

C. Guardiani, P. McNamara, L. Daldoss, S. Saxena, S. Zanella, W. Xiang, S. Liu

March 2002 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(172.01 KB) Publisher Site

Additional Information: full citation, abstract

In this paper, we present an innovative methodology toestimate and improve the quality of analog and mixed-signal circuit testing. We first detect and reduce the redundancy in the electrical test measurements (e-tests), then weidentify the e-test acceptability regions by considering performance specifications as well as process parameter distributions. Finally, we provide an effective metric for theaccurate assessment of the parametric test coverage ofembedded analog IP. Experimental results con ...

2 Models and metrics of interconnect performance: Investigating the frequency dependence elements of CMOS RFIC interconnects for physical modeling

B. H. Ong, C. B. Sia, K. S. Yeo, J. G. Ma, M. A. Do, E. P. Li

February 2004 **Proceedings of the 2004 international workshop on System level interconnect prediction**

Full text available: pdf(488.40 KB) Additional Information: full citation, abstract, references, index terms

Various structures of on-wafer interconnect for CMOS RFICs fabricated by using 0.18um CMOS are investigated experimentally. The measured S-parameters in terms of the dimensions and frequencies are presented in the paper. Frequency dependence elements of interconnect is extracted from the measurement. A scalable physical model is derived and quantified using measurement results for straight top-metal interconnect.

Keywords: distributed effects, frequency dependence elements, physical model, skin effects

3 An efficient statistical analysis methodology and its application to high-density DRAMs

Sang-Hoon Lee, Chang-Hoon Choi, Jeong-Taek Kong, Wong-Seong Lee, Jei-Hwan Yoo

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(161.64 KB) Publisher Site

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In this work, a new approach for the statistical worst case of full-chip circuit performance

and parametric yield prediction, using both the Modified-Principal Component Analysis (MPCA) and the Gradient Method (GM), is proposed and verified. This method enables designers not only to predict the standard deviations of circuit performances but also track the circuit performances associated with the process shift by measuring E-tests. This new method is validated experimentally during the developme ...

Keywords: Design for Manufacturing , statistical SPICE modeling, Principal Component Analysis, Gradient Method, High-Density DRAMs

4 CMU-CAM system
Andrzej J. Strojwas
June 1985 **Proceedings of the 22nd ACM/IEEE conference on Design automation**

Full text available: pdf(811.28 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper describes a software system for Computer Aided Manufacturing (CAM) of VLSI circuits being developed at Carnegie-Mellon University. In developing the system, a major effort was devoted towards the computational efficiency of the algorithms implemented. The results obtained with this system indicate that it can be used for a variety of real-life tasks, such as optimal process design, process diagnosis and control, in commercial fabrication lines. We believe that such a system provi ...

5 Modeling and simulation of high-frequency integrated circuits based on scattering parameters
A. T. Yang, C. H. Chan, J. T. Yao, R. R. Daniels, J. P. Harrang
June 1991 **Proceedings of the 28th conference on ACM/IEEE design automation**

Full text available: pdf(622.93 KB) Additional Information: full citation, references, citings, index terms

6 Model order-reduction of RC(L) interconnect including variational analysis
Ying Liu, Lawrence T. Pileggi, Andrzej J. Strojwas
June 1999 **Proceedings of the 36th ACM/IEEE conference on Design automation**

Full text available: pdf(63.59 KB) Additional Information: full citation, references, citings, index terms

7 Testing and Fault-Tolerance: Test generation for resistive opens in CMOS
Arun Krishnamachary, Jacob A. Abraham
April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**

Full text available: pdf(100.35 KB) Additional Information: full citation, abstract, references, index terms

This paper develops new techniques for detecting both stuck-open faults and resistive open faults, which result in increased delays along some paths. The improved detection of CMOS open defects is made possible by a new delay fault model which combines the advantages of the gate delay fault model and the path delay fault model. We develop a test generation methodology for this fault model which enables generation of test vectors that test a percentage of the longest sensitizable paths in the des ...

Keywords: defect detection, delay testing, resistive opens

8 Influence of manufacturing variations in IDDQ measurements: a new test criterion
Juan M. Díez, Juan C. López
January 2000

Proceedings of the conference on Design, automation and test in Europe

Full text available: pdf(128.07 KB) Publisher Site Additional Information: full citation, references, citings, index terms

9 Issues in timing analysis: Statistical gate delay model considering multiple input switching

Aseem Agarwal, Florentin Dartu, David Blaauw
June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(184.94 KB) Additional Information: full citation, abstract, references, index terms

There is an increased dominance of intra-die process variations, creating a need for an accurate and fast statistical timing analysis. Most of the recent proposed approaches assume a Single Input Switching model. Our experiments show that SIS underestimates the mean delay of a stage by upto 20% and overestimates the standard deviation upto 26%. We also show that Multiple Input Switching has a greater impact on statistical timing, than regular static timing analysis. Hence, we propose a modeling ...

10 A flexible statistical model for CAD of submicrometer analog CMOS integrated circuits

Christopher Michael, Christopher Abel, C. S. Teng
November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(363.42 KB) Additional Information: full citation, references, citings

11 Highlights of CMU research on CAD, CAM and CAT of VLSI circuits

John Paul Shen
November 1999 **Proceedings of 1986 ACM Fall joint computer conference**

Full text available: pdf(1.35 MB) Additional Information: full citation, references, index terms

12 A statistical performance simulation methodology for VLSI circuits

Michael Orshansky, James C. Chen, Chenming Hu
May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(243.16 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

A statistical performance simulation (SPS) methodology for VLSI circuits is presented. Traditional methods of worst-case corner analysis lack accuracy and Monte-Carlo simulations cannot be applied to VLSI circuits because of their complexity. SPS methodology is accurate because no statistical information about the device parameter variation is lost. It achieves efficiency by analyzing the smaller circuit blocks and generating the performance distribution for the entire circuit. Circuit eval ...

Keywords: custom sizing, migration, timing optimazation

13 Hierarchical statistical characterization of mixed-signal circuits using behavioral modeling

Eric Felt, Stefano Zanella, Carlo Guardiani, Alberto Sangiovanni-Vincentelli
January 1997 **Proceedings of the 1996 IEEE/ACM international conference on**

Computer-aided design

Full text available: pdf(231.06 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

A methodology for hierarchical statistical circuit characterization which does not rely upon circuit-level Monte Carlo simulation is presented. The methodology uses principal component analysis, response surface methodology, and statistics to directly calculate the statistical distributions of higher-level parameters from the distributions of lower-level parameters. We have used the methodology to characterize a folded cascode operational amplifier and a phase-locked loop. This methodology permi ...

Keywords: statistical characterization, mixed-signal circuits, behavioral modeling

14 Metrics, techniques and recent developments in mixed-signal testing

Gordon W. Roberts

January 1997 **Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(240.28 KB) Publisher Site Additional Information: full citation, abstract, references, index terms

This paper presents a tutorial on mixed-signal testing. Our focus is on testing the analog portion of the mixed-signal device, as the digital portion is handled in the usual way. We begin by first outlining the role of test in a manufacturing environment, and its impact on product cost and quality. We look at the impact of manufacturing defects on the behavior of digital and analog circuits. Subsequently, we argue that analog circuits require very different test methods than those presently used ...

Keywords: manufacturing defects, manufacturing environment, measurement setups, mixed analogue-digital integrated circuits, mixed-signal testing, product cost, quality

15 Design for manufacturability and yield

A. J. Strojwas

June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**

Full text available: pdf(700.12 KB) Additional Information: full citation, abstract, references, citings, index terms

This tutorial focuses on the design strategies for VLSI circuits that are aimed at achieving manufacturable, high-yielding chips. We review the current status of statistical design methodologies based upon statistically-valid modeling and process characterization approaches. Both parametric and functional yield maximization strategies are covered. This tutorial argues that by providing a better starting point for manufacturing, the profitability and competitiveness can be significantly impr ...

16 Testing and Debugging Custom Integrated Circuits

Edward H. Frank, Robert F. Sproull

December 1981 **ACM Computing Surveys (CSUR)**, Volume 13 Issue 4

Full text available: pdf(2.25 MB) Additional Information: full citation, references, citings, index terms

17 The impact of intra-die device parameter variations on path delays and on the design for yield of low voltage digital circuits

M. Eisele, J. Berthold, D. Schmitt-Landsiedel, R. Mahnkopf

August 1996 **Proceedings of the 1996 international symposium on Low power**

electronics and design

Full text available: pdf(343.57 KB) Additional Information: full citation, references, citings, index terms

18 Design-manufacturing interface: Part II - applications

W. Maly, H. T. Heineken, J. Khare, P. K. Nag, P. Simon, C. Ouyang

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(75.88 KB) Additional Information: full citation, abstract, references, citings, index terms

Publisher Site

This paper illustrates via examples problems at the design-manufacturing interface that exist in the IC industry today, and the ability of the YAN/PODEMA framework in solving these problems. The need for further development of the framework is also emphasized.

Keywords: manufacturability, yield, critical area, metal utilization, etch rate variation, antenna effect

19 Performance - manufacturability tradeoffs in IC design

H. T. Heineken, W. Maly

February 1998 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(64.48 KB) Additional Information: full citation, abstract, references, citings, index terms

Publisher Site

Traditional VLSI design objectives are to minimize time-to-first-silicon while maximizing performance. Such objectives lead to designs which are not optimum from a manufacturability perspective. The objective of this paper is to illustrate the above claim by performing performance/ manufacturability tradeoff analysis. The basis for such an analysis, in which the relationship between a product's clock frequency and wafer productivity is modeled, is described in detail. New applied yield models ar ...

Keywords: manufacturability, wafer productivity, performance, clock frequency, critical area, yield, design rule shrink

20 (Special session) embedded tutorial: RF modeling and design methodology: RF design methodologies bridging system-IC-module design

Robert A. Mullen

January 2004 **Proceedings of the 2004 conference on Asia South Pacific design automation: electronic design and solution fair 2004**

Full text available: pdf(538.14 KB) Additional Information: full citation, abstract, references

There has been a long-standing need to link the RF design domains into a connected, common design environment. Such a methodology is possible through implementing system-level behavioral models with different levels of abstraction that can be modeled or co-simulated at the IC circuit level. At module or board design, it is possible to link and simulate multiple chips with board-level components and parastics in an RFIC design environment.With today's more complex IC designs that are heading towa ...